The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-6. (Canceled)

7. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a source follower circuit comprising an n-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the n-channel thin film transistor comprises a polycrystalline semiconductor,

the n-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the n-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2, and~~

an active layer of the n-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, phosphorous is used to the n-channel thin film transistor.

8. (Previously Presented) The driver circuit according to claim 7,

wherein the n-channel thin film transistor is directly connected to an output terminal.

9. (Original) The driver circuit according to claim 7,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

10. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a source follower circuit comprising an n-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the n-channel thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon,

the n-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the n-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2; and~~

an active layer of the n-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, phosphorous is used to the n-channel thin film transistor.

11. (Previously Presented) The driver circuit according to claim 10,

wherein the n-channel thin film transistor is directly connected to an output terminal.

12. (Original) The driver circuit according to claim 10,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

13. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a bootstrap circuit comprising an n-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the n-channel thin film transistor comprises a polycrystalline semiconductor,

the n-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the n-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2, and~~

an active layer of the n-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, phosphorous is used to the n-channel thin film transistor.

14. (Previously Presented) The driver circuit according to claim 13,

wherein the n-channel thin film transistor is directly connected to an output terminal.

15. (Original) The driver circuit according to claim 13,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

16. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a bootstrap circuit comprising an n-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the n-channel thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon,

the n-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the n-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2, and~~

an active layer of the n-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, phosphorous is used to the n-channel thin film transistor.

17. (Previously Presented) The driver circuit according to claim 16,

wherein the n-channel thin film transistor is directly connected to an output terminal.

18. (Original) The driver circuit according to claim 16,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

19.-24. (Canceled)

25. (Previously Presented) The driver circuit according to claim 7, wherein the semiconductor layer of the n-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

26. (Previously Presented) The driver circuit according to claim 10, wherein the semiconductor layer of the n-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

27. (Previously Presented) The driver circuit according to claim 13, wherein the semiconductor layer of the n-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

28. (Previously Presented) The driver circuit according to claim 16, wherein the semiconductor layer of the n-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

29. (Previously Presented) The driver circuit according to claim 25, wherein the metal element is nickel.

30. (Previously Presented) The driver circuit according to claim 26, wherein the metal element is nickel.

31. (Previously Presented) The driver circuit according to claim 27, wherein the metal element is nickel.

32. (Previously Presented) The driver circuit according to claim 28, wherein the metal element is nickel.

33. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a source follower circuit comprising a p-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the p-channel thin film transistor comprises a polycrystalline semiconductor,

the p-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the p-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2, and~~

an active layer of the p-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, boron is used to the p-channel thin film transistor.

34. (Previously Presented) The driver circuit according to claim 33,

wherein the p-channel thin film transistor is directly connected to an output terminal.

35. (Previously Presented) The driver circuit according to claim 33,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

36. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a source follower circuit comprising a p-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the p-channel thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon,

the p-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the p-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2;~~ ~~and~~

an active layer of the p-channel thin film transistor contains an impurity at a concentration in a range of 5 x 10^{12} to 5 x 10^{14} atoms/cm^2, and

as for the impurity, boron is used to the p-channel thin film transistor.

37. (Previously Presented) The driver circuit according to claim 36,

wherein the p-channel thin film transistor is directly connected to an output terminal.

38. (Previously Presented) The driver circuit according to claim 36,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

39. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a bootstrap circuit comprising a p-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the p-channel thin film transistor comprises a polycrystalline semiconductor,

the p-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the p-channel thin film transistor at a concentration not greater than 5 x 10^{14} atoms/cm^2;~~ ~~and~~

an active layer of the p-channel thin film transistor contains an impurity at a concentration in a range of 5×10^{12} to 5×10^{14} atoms/cm^2, and

as for the impurity, boron is used to the p-channel thin film transistor.

40. (Previously Presented) The driver circuit according to claim 39,

wherein the p-channel thin film transistor is directly connected to an output terminal.

41. (Previously Presented) The driver circuit according to claim 39,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

42. (Currently Amended) A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the shift register, comprising a bootstrap circuit comprising a p-channel thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the p-channel thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon,

the p-channel thin film transistor is a depletion mode transistor,

~~an impurity is doped to a channel forming region of a semiconductor layer of the p-channel thin film transistor at a concentration not greater than 5×10^{14} atoms/cm^2, and~~

an active layer of the p-channel thin film transistor contains an impurity at a concentration in a range of 5×10^{12} to 5×10^{14} atoms/cm^2, and

as for the impurity, boron is used to the p-channel thin film transistor.

43. (Previously Presented) The driver circuit according to claim 42,

wherein the p-channel thin film transistor is directly connected to an output terminal.

44. (Previously Presented) The driver circuit according to claim 42,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

45. (Previously Presented) The driver circuit according to claim 33, wherein the semiconductor layer of the p-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

46. (Previously Presented) The driver circuit according to claim 36, wherein the semiconductor layer of the p-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

47. (Previously Presented) The driver circuit according to claim 39, wherein the semiconductor layer of the p-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

48. (Previously Presented) The driver circuit according to claim 42, wherein the semiconductor layer of the p-channel thin film transistor comprises a metal element which is capable of promoting the crystallization of a semiconductor film.

49. (Previously Presented) The driver circuit according to claim 45, wherein the metal element is nickel.

50. (Previously Presented) The driver circuit according to claim 46, wherein the metal element is nickel.

51. (Previously Presented) The driver circuit according to claim 47, wherein the metal element is nickel.

52. (Previously Presented) The driver circuit according to claim 48, wherein the metal element is nickel.